CLAIMS

1. A method of manufacturing a vertical insulated gate transistor comprising the steps of:

providing a semiconductor body (1) having opposed first (10) and second (12) major surfaces;

forming a trench (26) extending vertically from the first major surface (10) towards the second major surface (12);

forming a gate dielectric layer (18) on the sidewalls and base of the trench;

depositing a conducting gate material layer (20) on the gate dielectric layer on the sidewalls and base of the trench;

carrying out a spacer etch to remove the gate material layer from the base of the trench leaving gate material on the sidewalls forming gate elements (21);

filling dielectric (30) into the trench between the sidewalls; and

forming a gate electrical connection layer (32) across the top of the trench electrically connecting the gate material layer across the trench.

2. A method of manufacturing a vertical insulated gate transistor according to claim 1 further comprising:

forming a hard mask (14) defining an opening (16) on the first major surface of the semiconductor body; and

etching the semiconductor body (1) through the opening (16) in the hard mask to pattern the trench (26).

3. A method according to claim 1 or 2 wherein the step of forming a gate electrical connection layer (32) includes covering the semiconductor body (1) with a conducting layer and patterning the gate electrical connection layer to span the trench above the first major surface and the dielectric.

4. A method according to any preceding claim wherein the step of filling dielectric into the trench includes the steps of depositing dielectric (30) and etching back the dielectric.

5. A method according to claim 4 wherein:

the step of etching back the dielectric defines a gap (40) at the top of the trench; and

the step of forming a gate electrical connection layer (32) includes depositing conducting material (32) on the first major surface (10) to fill the gap and to define a plug (42) at the top of the trench and planarising the gate electrical connection layer (32) to remove the electrical connection layer (32) from the first major surface but to leave the plug (42) in the trench in place.

6. A method according to any preceding claim further comprising the steps of:

depositing a gate-source insulating layer (44) over the trench (26) to isolate the gate electrical connection layer (32); and

depositing a source conducting layer (46) over the gate source insulating layer (44) and the first major surface (10) so that the source conducting layer (46) is in electrical contact with the semiconductor body (1) but insulated from the gate electrical connection layer (32).

7. A semiconductor device, comprising:

a semiconductor body (1) having opposed first and second major surfaces (10, 12), the semiconductor body (1) having a highly doped drain layer (2) of a first conductivity type and lower doped body layer (6) on the highly doped layer facing the first major surface (10);

a trench (26) extending into the semiconductor body (1) from the first major surface (10) defining opposed sidewalls (22) and a base (24);

a source region (8) of the first conductivity type laterally adjacent to the trench (26) at the first major surface;

a gate dielectric (18) on the sidewalls and base of the trench;

opposed gate elements (21) on the sidewalls (22) of the trench but not on the base of the trench (24);

an insulating filler (30) extending upwards from the base (24) of the trench between the gate elements (21); and

a gate electrical connection layer (32) at the top of the trench (26) above the insulating filler (30), the gate electrical connection layer (32) connecting the gate elements (21) across the trench (26).

8. A semiconductor device according to claim 7 wherein the top of the insulating filler (30) is level with the top of the trench (26) and the gate electrical connection layer (32) extends across the top of the trench (26) above the filler (30).

9. A semiconductor device according to claim 8 wherein the gate electrical connection layer is a plug (40) in the trench above the insulating filler (30).

10. A semiconductor device according to claim 9 wherein the top of the plug (40) is planarised to be level with the top of the trench (26).

11. A semiconductor device according to any of claims 7 to 10 further comprising a gate-source dielectric isolation layer (44) above the gate electrical connection layer and a source conducting layer (46) isolated from the gate electrical connection layer by the gate-source dielectric isolation layer and in contact with the source region.

12. A semiconductor device according to any of claims 7 to 11 further comprising:

a low doped drain layer (4) over the highly doped drain layer (2) and underneath the body layer (6), the trench extending through the body layer (6) into the low doped drain layer (4); and

a dielectric plug (50) at the base of the trench (26).